In re Patent Application of:
BAHOUT
Serial No. **10/081,740**
Filing Date: **FEBRUARY 22, 2002**

REMARKS

The Applicant would like to thank the Examiner for the thorough examination of the present application. The claim objections have been corrected as helpfully suggested by the Examiner. The arguments supporting patentability of the claimed invention are presented below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 7, 11, 17 and 25 over the article by Greenfield et al. titled "Using Microprocessors and Microcomputers: The 6800 Family." The Examiner also rejected independent Claim 21 over the Greenfield et al. article in view of the Nakagawa et al. patent. The rejection of independent Claim 21 will also be discussed herein.

The present invention, as recited in independent Claim 17, for example, is directed to a device for reading sequentially from a memory, wherein the device comprises an input register containing an instruction code and a memory address code, and an incremental address counter having an input connected to the input register for receiving the memory address code therefrom and an output connected to the memory. An output register has an input connected to the memory for recording contents read at the memory address code indicated by the incremental address counter. An address jump detection circuit has an input connected to the input register for detecting an address jump instruction code, and an output connected to the incremental address counter for supplying an increment signal thereto. A transfer circuit is connected to the incremental address counter and to the output register for

transferring the recorded contents read at the incremented address to the incremental address counter.

The device in accordance with the claimed invention advantageously provides for the sequential readout of a memory in which address jumps are very fast. This is accomplished by sending to the memory not a complete message but rather an instruction code, i.e., without an address, so that the instruction code is interpreted by the memory as indicating that the new address is to use the value of the word contained at the following address. This avoids sending to the device a new message that contains both a jump instruction and a new address.

Independent Claim 21 is similar to independent Claim 17 except the transfer circuit has been replaced with a logic gate and a multiplexer circuit. Independent Claim 25 is similar to independent Claim 17 except this claim further recites a microprocessor connected to the input register for providing the instruction code and memory address code thereto.

Independent method Claim 11 is similar to independent device Claim 17. Independent method Claim 7 is similar to independent method Claim 11 except this claim recites an address jump signal incrementing the incremental address counter instead of an instruction code or a memory address code.

Referring now to the Greenfield et al. article, a Motorola 6800 microprocessor instruction set which includes a JUMP instruction is disclosed. The Examiner has taken the position that the data buffer in FIG. 8-3 represents the input register receiving an instruction code and a memory address

code. Since the JUMP address value (FIG. 6-1b) is loaded into a PC, the Examiner has characterized the PC as an incremental address counter that is connected to the input register and to an output register (i.e., output buffer) via an 8-bit internal bus. The contents of the instruction read at K can be read from a RAM.

The Greenfield et al. article further discloses that the JUMP instruction is decoded to determine that a JUMP instruction is being executed, where the instruction decoder is coupled to the output registers. The Examiner further states that since a JUMP extended instruction has been decoded, the disclosed 6800 microprocessor knows that the PC is incremented to read the high and low address bytes of the "JUMP to" address. Greenfield et al. further discloses that the 8-bit internal bus interfaces with 3-state output devices so that these devices can communicate with one another over the common bus.

The Applicant respectfully submits that the Examiner has mischaracterized the Greenfield et al. article, particularly with respect to the transfer circuit transferring the recorded contents read at the incremented address to the incremental address counter. In FIG. 8-3 of the Greenfield et al. article, an 8-bit internal bus connects the various registers with the instruction decode and control logic. Reference is directed to page 180, section 8-5.4 of Greenfield et al., which provides:

> "An interrupt is a signal to the μP that causes it to stop execution of the normal program and to branch (or jump) to another location that is the beginning address of

> an interrupt service routine. These routines are written to provide whatever action is necessary to respond to the interrupt."

Reference is also directed to page 116, section 6-3.1 of Greenfield et al., which provides:

> "Extended jumps are three-byte instructions, where the last two bytes are a 16-bit address. Their action is shown in Fig. 6-1b. Since a 16-bit address is available, they allow the program to jump to any location in memory." (Emphasis added.)

The Applicant submits that Greenfield et al. fails to disclose a transfer circuit connected to the incremental address counter (which the Examiner characterized as the PC) and to the output register for transferring the recorded contents read at the incremented address to the incremental address counter. In Greenfield et al., the extended JUMP includes an address associated therewith, i.e., "the last two bytes are a 16-bit address."

In sharp contrast, the claimed invention sends to the memory not a complete message but rather an instruction code, i.e., without an address, so that the instruction code is interpreted by the memory as indicating that the new address is to use the value of the word contained at the following address. This avoids sending to the device a new message that contains both a jump instruction and a new address. Consequently, the transfer circuit as recited in independent Claim 17 transfers the recorded contents read at the incremented address to the incremental address counter.

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Therefore, the Applicant submits that independent Claim 17 is patentable over the Greenfield et al. article. Independent Claims 7, 11 and 25 are similar to independent Claim 17, and it is submitted that these claims are also patentable over the Greenfield et al. article. Since the Nakagawa et al. patent fails to provide the noted deficiencies with respect to the Greenfield et al. article, the Applicant submits that independent Claim 21 is patentable over the Greenfield et al. article in view of the Nakagawa et al. patent. In view of the patentability of independent Claims 7, 11, 17, 21 and 25, their respective dependent claims, which recite yet further distinguishing features, are also patentable, and require no further discussion herein.

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CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 9th day of November, 2004.